REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 19 October 2005. Responsive to the rejection made in the Official Action, Independent Claims 1, 5 and 9 have been amended to clarify the combination of elements defining the novel concept of the present invention.

In the Official Action, Claims 1 – 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lowe, U.S. Patent 6,058,253. Prior to discussion of the cited reference and the distinguishing features between the prior art and the present invention, it is believed that a brief discussion of the novel concept disclosed in the present Patent Application will facilitate the prosecution of the Patent Application in question.

The present invention is a testing device allowing to test a plurality of peripheral devices, each having a USB interface. The testing device of the present invention includes a CPU (central processing unit), a memory either directly coupled to the CPU or included into the CPU, and a control chip equipped with the USB interface control and having a plurality of connecting ports for connecting with the plurality of peripheral devices for providing simultaneous testing thereof, if needed.

The memory includes a firmware program as well as test packets, to test the plurality of the peripheral devices under the test through the control chip.

The communication between the peripheral devices and the testing device is through the USB (Universal Serial Bus). For this purpose, the USB interface is

provided in each of the peripheral devices, and the USB interface is included in the control chip 26.

Turning now to the Lowe, the reference cited by the Examiner, this is directed to a method and an apparatus for intrusive testing of a microprocessor feature. Microprocessor testing system includes a central processing unit (CPU) 30 coupled to Chip Set Logic 32. Chip Set Logic 32 is coupled to a system bus 34 and a memory bus 36. A memory unit 38 is coupled to memory bus 36. A peripheral device 40 may be coupled to system bus 34. The CPU 30 obtains data from the memory unit 38 via chip set logic 32, and stores data to memory unit 38 via chip set logic 32. Chip set logic 32 functions as interface between CPU 30 and system bus 34, and between CPU 30 and memory unit 38. Peripheral device 40 may be a disc drive unit, video display unit, or a printer. Memory unit 38 includes microprocessor test group 10. The microprocessor test group 10 includes software implementation of the microprocessor module 12. During use, microprocessor module 12 is caused to execute a testing program. The testing program includes a set of instructions which require cooperation of the feature and produce a result. The result produced by the microprocessor module is compared to an expected result. Any difference between the result produced by the microprocessor module and the expected result may indicate an error in feature hardware or in the control circuitry of the feature.

It is respectfully submitted, that Lowe fails to suggest, disclose or render obvious the structure which the Applicant regards as the invention. Specifically,

A. Lowe is a device for testing a microprocessor, e.g. the structure, as best shown in figures 3 and 4, internal to the testing device itself. Lowe, in contrast to the present invention, is not concerned with testing of a peripheral device 40 whatsoever. As a matter of fact, the reason for coupling the peripheral device 40 to the testing device is not clear, as the peripheral device 40 is not part of the testing procedure described in Lowe's Patent.

As Lowe is not intended for testing the peripheral devices, it fails to suggest, disclose or render obvious the peripheral devices under the test, or sending the test packets to the peripheral devices, or that the peripheral devices, upon receiving the test packet, send the test packet back to the CPU for determining whether the test packet has not been changed during the testing procedure.

While in the present invention, the testing device is clearly for testing a plurality of peripheral devices coupled to the testing device. The testing procedure of the present invention is designed for testing the peripheral devices under the test, and therefore comprises transmission of the test packets to the peripheral devices under the test, so that the same could send the received test packets back to the CPU for further analysis.

This feature is completely missing from the Lowe reference.

B. In contrast to the present invention, nowhere in the Lowe Patent, it is presented that the system bus 34 is a Universal Serial Bus (USB). Neither it is taught in Lowe that the peripheral device 40 is provided with the USB interface,

nor that the Chip Set Logic 32 communicates with the system bus 34 through the USB interface.

While in the present invention, each of the plurality of peripheral devices under the test is equipped with the USB interface. The control chip also includes a USB interface control. These features are completely missing in Lowe.

C. In Lowe, the CPU 30 is coupled to the memory unit 38 through the Chip Set Logic 32 which function, as the interface between the CPU 30 and system bus 34, and between CPU 30 and the memory unit 38. The Chip Set Logic 32 includes a memory controller.

In contrast to Lowe, in the present invention, the memory 22 is either directly coupled to the CPU 24 or is included into the CPU.

D. Further, in Lowe, in contrast to the present invention, the chip set logic 32 fails to be provided with a plurality of connecting ports for connecting with the plurality of peripheral devices.

While in the present invention the control chip 26 has a plurality of connecting ports for connecting with peripheral devices under the test.

Claim 1, as amended, includes (inter alia) the following limitations:

"... a memory ... being connected directly to said CPU ..."

"... a control chip including USB interface control and having a plurality of connecting ports for connecting with said plurality of peripheral devices under the test ...".

These features, which are emphasized in Claim 1, as amended, are clearly missing from the Lowe reference.

Claim 5, which is directed to a testing device for testing of at least one peripheral device, includes (among others) the following limitations:

"... a CPU having a memory ..."

"a control chip with USB interface ..."

"... wherein said control chip is provided with a plurality of connecting ports for connecting with said at least one peripheral device under the test ...".

Claim 9 is directed to a testing device for testing of at least one peripheral device and includes (inter alia) the following limitations:

"... a CPU directly connected with at least one memory ..."

"a control chip with USB interface control ..."

"wherein said CPU sends a test packet stored in the memory to said at lest one peripheral device under the test ..."

"wherein ... said at least one peripheral device under the test sends said test packet back to said CPU ...".

As Lowe fails to disclose each and every one of the claimed elements, it cannot anticipate the invention of the subject Patent Application, as now claimed in claims 1, 5 and 9. Therefore, the allowance of Claims 1, 5 and 9 is believed; and the same is respectfully requested.

Claims 3 – 4 and 6 – 8 have been amended to improve the claim language thereof.

Claims 2 – 4, dependent (directly or indirectly) upon Claim 1, and Claims 6 – 8, dependent (directly or indirectly) upon Claim 5, are believed each to add further limitations that are patentably distinct in addition to be dependent upon what is now believed to be patentable base claim, and therefore, allowable for at least the same reasons.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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